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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/808,750
Filing Date: March 15, 2001
Appellant(s): VO, HUY THANH

Timothy Clise
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/09/06 appealing from the Office action mailed 01/30/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,940,315	COWLES	08-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-4, 8-14, 15-18, 26-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Cowles (U.S. Patent 5,940,315).

Regarding claim 1, Cowles discloses a memory array (figure 2A), comprising: a number of memory cells (not shown. At column 1, lines 28-38, Cowles teaches each cell has a gate region connected to a wordline, a drain connected to a bit line and a source connected to a capacitor) having a first source/drain region and a second source/drain region and a gate region; a number of source lines (not shown) coupled to the first source/drain region of at least one memory cell; a number of bit lines (not shown) coupled to the second source/drain region of at least one memory cell; a number of wordlines (30-33) coupled to the gate region of at least one memory cell; a strapping line (112) of lower resistance than the wordlines coupled to a single continuous wordline (31) in a single array (memory bank 100) wherein the strapping line bypasses only a portion in a middle region between a first and second end of the single continuous wordline, and wherein the strapping line is spaced apart from adjacent conductive

structures by a distance greater than a wordline pitch (figure 2B shows that distance between strapping lines 112 and 113 is greater than a wordline pitch between wordlines 31 and 32); and wherein the strapping line (112) bypasses only a portion a wordline within the single memory array (memory bank 100) and bypasses a different portion of a wordline within the single array than an adjacent strapping line (Figure 2A shows strapping line 112 bypasses a different portion of a wordline than strapping lines 110 or 111); and at least two channels (such as node 150 in figure 2A) connecting the strapping line to a first and second end of the portion of the single wordline.

Regarding claim 2, Cowles also teaches that the strapping line comprises metal (column 4, lines 5-11).

Regarding claim 3, Cowles also teaches the strapping line metal comprises a refractory metal (tungsten and titanium are refractory metals; column 4, lines 5-11).

Regarding claim 4, Cowles teaches that the portion of the wordline bypassed by the strapping line comprises a first half of the memory cells coupled to the wordline (two middle memory arrays in figure 2A are considered as a first half of the memory cells).

Regarding claim 8, Cowles discloses a memory device, comprising: a number of memory cells (not shown but inherent in a DRAM device) having a first source/drain region and a second source/drain region and a gate region, the memory cells forming a memory cell array; a number of source lines (not shown but inherent as lines connected to capacitors in a DRAM) coupled to the first source/drain region of at least one memory cell; a number of bit lines (not shown but inherent as bit lines in a DRAM) coupled to the second source/drain region of at least one memory cell; a single array (arrays 20-23 in

figure 2A are considered a single array for this rejection) of parallel wordlines (30-33) coupled to the gate region of at least one memory cell (as shown in figure 4 of the instant application), the array of parallel wordlines having a pitch (space between word lines 31 and 32 in figure 2B); a number of strapping devices (110 to 115 in figure 2A) which bypass portions of the wordlines in the single array of parallel wordlines, wherein at least one portion of a single continuous wordline is only in a middle region (strapping device 112) between a first and second end of the single continuous wordline, and wherein adjacent strapping devices bypass only a portion (strapping device 110) of a wordline within the memory array and bypass different portions of adjacent wordlines within the memory array, each strapping device (110-115) comprising: a strapping line of lower resistance than the wordlines (column 4, lines 9-11), wherein the strapping lines are each located a distance from each other that is greater than the pitch (figure 2B shows a distance between strapping lines 112 and 113 being greater than the pitch between word lines 31 and 32); and at least two channels (at nodes such as node 150 in figure 2A) connecting each strapping line to a portion of a single wordline.

Regarding claim 9, Cowles teaches the memory device of claim 8 wherein the strapping line comprises metal (column 4, lines 5-11).

Regarding claim 10, Cowles teaches the memory device of claim 9 wherein the metal comprises a refractory metal (tungsten and titanium are refractory metals; column 4, lines 5-11).

Regarding claim 11, Cowles teaches the memory device of claim 8 wherein the portions of the wordlines in the array bypassed by the number of strapping devices

comprises a plurality of end portions of the wordlines (figure 2A shows at nodes such as node 150 wordlines have a plurality of end portions).

Regarding claim 12, Cowles shows in figure 2A, the strapping devices (110 and 111) are located on alternating wordlines in the array.

Regarding claim 13, Cowles shows in figure 2A, the strapping devices (110, 112) are located on adjacent wordlines and staggered along the wordlines such that the portions of the adjacent wordlines that are bypassed are not adjacent to each other.

Regarding claim 14, Cowles shows in figure 2A, the strapping devices (110 to 115) strap a first half portion (arrays 21 and 22) of a number of even wordlines in the array and a second half portion (arrays 20 and 23) of a number of odd wordlines.

Regarding claim 15, Cowles teaches an integrated circuit (figure 2A) comprising: at least one memory array (20-23) comprising: a number of memory cells (not shown but inherent in a DRAM device) having a first source/drain region and a second source/drain region and a gate region; a number of source lines (not shown) coupled to the first source/drain region of at least one memory cell; a number of bit lines (not shown) coupled to the second source/drain region of at least one memory cell; a number of wordlines (30, 31 in figure 2A) in a single array (arrays 20-23 are considered as a single array) coupled to the gate region of at least one memory cell; a strapping line (112) of lower resistance than the wordlines (column 4, lines 9-11) coupled to a single continuous wordline (31) wherein the strapping line (112) bypasses only a portion of the wordline within the memory array in a middle region between a first and second end of the single continuous wordline, wherein the strapping line (112) is spaced apart

from adjacent conductive structures (113 in figure 2B) by a distance greater than a wordline pitch (a space between 112 and 113 is greater than a space between 31 and 32), and wherein the strapping line (112) bypasses a different portion of a wordline within the memory array than an adjacent strapping line (110 or 111 in figure 2A); at least two channels (at nodes such as node 150 in figure 2A) connecting the strapping line to a first and second end of the portion of the single continuous wordline (31); a row decoder (50 in figure 2A); a column decoder (40); and a sense amplifier (column 1, lines 35-38).

Regarding claim 16, Cowles teaches the integrated circuit of claim 15 wherein the strapping line comprises metal (column 4, lines 5-11).

Regarding claim 17, Cowles teaches the integrated circuit of claim 16 wherein the metal comprises a refractory metal (tungsten and titanium are refractory metals; column 4, lines 5-11).

Regarding claim 18, Cowles shows in figure 2A, the portion of the wordline bypassed by the strapping line (112) comprises a first half of the memory cells coupled to the wordline (a second half of the memory cells is in arrays 20 and 23).

Regarding claims 26-29, Cowles shows in figure 3, information handling device comprising: a processing unit (334); at least one memory array (348). The limitations of the memory array are discussed in claims 15-18.

Claims 5-7, 19-25, 30-36, 37-41, 45-48, and 49-54 are rejected under 35 U.S.C. 102(b) as being anticipated by Cowles (U.S. Patent 5,940,315).

Regarding claim 5, Cowles discloses a memory array (figures 2A, 2B) comprising: a number of memory cells (not shown. At column 1, lines 28-38, Cowles teaches each cell has a gate region connected to a wordline, a drain connected to a bit line and a source connected to a capacitor) having a first source/drain region and a second source/drain region and a gate region; a number of source lines (not shown) coupled to the first source/drain region of at least one memory cell; a number of bit lines (not shown) coupled to the second source/drain region of at least one memory cell; a number of wordlines (30-33 in figure 2A) coupled to the gate region of at least one memory cell; a plurality of separate strapping lines (110-115) of lower resistance than the wordlines (column 4, lines 5-11) coupled to at least one of the number of wordlines (wordline 31) in a single array (memory block 100 in figure 2A) wherein the strapping lines bypass a plurality of separate portions of a single continuous wordline (column 3, lines 57-60), and wherein adjacent strapping lines (110, 112) bypass only a portion of a wordline within the memory array and bypass different portions of adjacent wordlines within the memory array (Figure 2A shows strapping line 112 bypasses a different portion of a wordline than strapping lines 110 or 111); and a plurality of channels (at nodes such as node 150 in figure 2A) connecting the plurality of strapping layers to the wordline.

Regarding claim 6, Cowles also teaches that the strapping line comprises metal (column 4, lines 5-11).

Regarding claim 7, Cowles also teaches the strapping line metal comprises a refractory metal (tungsten and titanium are refractory metals; column 4, lines 5-11).

Regarding claim 19, Cowles teaches an integrated circuit (figure 2A) comprising: at least one memory array (memory bank 100) comprising: a number of memory cells (not shown) having a first source/drain region and a second source/drain region and a gate region; a number of source lines coupled to the first source/drain region of at least one memory cell; a number of bit lines coupled to the second source/drain region of at least one memory cell; a single array of parallel wordlines (30-33) coupled to the gate region of at least one memory cell, the array of parallel wordlines having a pitch (space between word lines 31 and 32 in figure 2B); a number of separate strapping devices (110-115) which bypass separate portions of a single continuous wordline in the single array of parallel wordlines, and wherein adjacent strapping devices (110 and 112) bypass only a portion of a wordline within the memory array and bypass different portions of adjacent wordlines within the single array, each strapping device (110-115) comprising: a strapping line of lower resistance than the wordlines (column 4, lines 5-11), wherein the strapping lines are each located a distance from each other that is greater than the pitch (figure 2B shows a distance between strapping lines 112 and 113 being greater than the pitch between word lines 31 and 32); and at least two channels (at nodes such as node 150 in figure 2A) connecting the strapping line to the single continuous wordline (31); a row decoder (50); a column decoder (40); and a sense amplifier (column 1, lines 35-38).

Regarding claim 20, Cowles teaches the integrated circuit of claim 15 wherein the strapping line comprises metal (column 4, lines 5-11).

Regarding claim 21, Cowles teaches the integrated circuit of claim 16 wherein the metal comprises a refractory metal (tungsten and titanium are refractory metals; column 4, lines 5-11).

Regarding claim 22, Cowles shows in figure 2A, the integrated circuit of claim 19 wherein the portions of the wordlines in the array bypassed by the number of strapping devices comprises a plurality of end portions of the wordlines.

Regarding claim 23, Cowles shows in figure 2A, the strapping devices (110 and 111) are located on alternating wordlines in the array.

Regarding claim 24, Cowles shows in figure 2A, the strapping devices (110, 112) are located on adjacent wordlines and staggered along the wordlines such that the portions of the adjacent wordlines that are bypassed are not adjacent to each other.

Regarding claim 25, Cowles shows in figure 2A, the strapping devices (110 to 115) strap a first half portion (arrays 21 and 22) of a number of even wordlines in the array and a second half portion (arrays 20 and 23) of a number of odd wordlines.

Regarding claims 30-36, Cowles teaches information handling device (figure 3) comprising: a processing unit (344); at least one memory array (348). The limitations of the at least one memory array are discussed in claims 19-25.

Regarding claim 37, Cowles discloses a method of reducing a wordline RC time constant (to minimize signal delays; column 1, lines 57-64) comprising: spacing a number of strapping devices (110-115 in figure 2A) over wordlines (30-33) within a

single memory array (memory bank 100) apart from adjacent strapping devices by a distance greater than a wordline pitch (figure 2B shows a distance between strapping lines 112 and 113 being greater than the pitch between word lines 31 and 32), wherein adjacent strapping devices bypass different portions of adjacent wordlines within the single memory array; connecting individual strapping devices (112 and 113) to portions in a middle region between a first and second end of single continuous wordlines (31 and 33) using at least two channels (at nodes 150) for each strapping device; activating a first number of transistors (transistors of memory cells connected to word line 31 in regions 21 and 22) coupled to a first portion of a wordline; and activating a second number of transistors (transistors of memory cells connected to the word line 31 in regions 20 and 23) coupled to a second portion of a wordline, wherein a signal used for activating the second number of transistors bypasses the first portion of the wordline through a strapping device of lower resistance than the first portion of the wordline (column 4, lines 12-19); activating a selected bitline in the memory array associated with a selected memory cell (column 1, lines 32-38); discharging the selected memory cell through a selected transistor, the selected transistor being activated by both the selected row and the selected bitline (column 1, lines 32-38); and sensing the presence or absence of a charge from the selected memory cell through the use of a sense amplifier (column 1, lines 32-38).

Regarding claim 38, Cowles discloses that activating a second number of transistors (transistors of memory cells connected to the word line 31 in regions 20 and 23 in figure 2A) coupled to a second portion of a wordline comprises: sending a signal

through a first channel to a metal strapping line (thru node 150 in figure 2A); sending the signal through the metal strapping line (112); and sending the signal through a second channel (at the other end of line 112) to the second portion of the wordline.

Regarding claim 39, Cowles teaches that sending the signal through the metal strapping line (112 in figure 2A) comprises sending the signal through a refractory metal strapping line (titanium and tungsten are refractory metals; column 4, lines 5-11).

Regarding claim 40, Cowles shows in figure 2A, activating a first number of transistors coupled to a first portion of a wordline (transistors of memory cells connected to the word line 31 in regions 21 and 22) comprises activating a first number of transistors coupled to a first half of the wordline.

Regarding claim 41, Cowles shows in figure 2A, activating a selected row (word line 31) in a memory array comprises bypassing multiple portions (in regions 21 and 22) of the wordline using multiple strapping devices (strapping line 112 has 1 portion in region 21 and a portion in region 22) of lower resistance than the wordline (column 4, lines 9-11).

Regarding claim 45, Cowles teaches a method of forming a memory device (figures 2A and 2B) comprising: forming a number of memory cells (not shown but understood as inherent in a semiconductor memory device; column 3, lines 22-33) having a first source/drain region and a second source/drain region and a gate region (such as a memory cell shown in figure 4 of the instant application), the memory cells forming a memory cell array (figure 2A); coupling a number of source lines to the first source/drain region of at least one memory cell (source terminals of transistors in figure

4 of the instant application are connected to a source line); coupling a number of bit lines to the second source/drain region of at least one memory cell (drain terminals of the transistors are connected to bit lines); attaching a number of wordlines to the gate region of at least one memory cell to form a single array (gate terminals of the transistors are connected to word lines); attaching a strapping line (112 in figure 2A) of lower resistance than the wordlines (column 4, lines 9-11) to a single continuous wordline (31 in figure 2A) wherein the strapping line bypasses only a portion in a middle region between a first and second end of the single continuous wordline, wherein the strapping line (112) is spaced apart from adjacent conductive structures (113) by a spacing greater than a wordline pitch (figure 2B shows a distance between strapping lines 112 and 113 being greater than the pitch between word lines 31 and 32) and wherein the strapping line (112) bypasses only a portion of a wordline within the memory cell array and bypasses a different portion of a wordline within the memory cell array than an adjacent strapping line (110 or 111); and connecting the strapping line (112) to the single wordline (31) by forming at least two channels (at nodes such as 150) from the strapping line to the single continuous wordline.

Regarding claim 46, Cowles discloses that attaching at least one strapping line (112) of lower resistance than the wordlines (column 4, line 9-11) to at least one of the number of wordlines comprises attaching at least one metal strapping line.

Regarding claim 47, Cowles teaches that attaching at least one metal strapping line (112) comprises attaching at least one refractory metal strapping line (titanium and tungsten are refractory metals; column 4, lines 5-11).

Regarding claim 48, Cowles discloses that attaching at least one strapping line (112) of lower resistance than the wordlines to at least one (31) of the number of wordlines comprises attaching multiple strapping lines (strapping line 112 has at least two portions: one in region 21 and one in region 22) to bypass multiple portions of a single wordline.

Regarding claim 49, Cowles teaches a method of forming a memory device (figure 2A) comprising: forming a number of memory cells (not shown but understood as inherent in a semiconductor memory device; column 3, lines 22-33) having a first source/drain region and a second source/drain region and a gate region (such as a memory cell shown in figure 4 of the instant application), the memory cells forming a memory cell array (figure 2A); coupling a number of source lines coupled to the first source/drain region of at least one memory cell (source terminals of transistors in figure 4 of the instant application are connected to a source line); coupling a number of bit lines coupled to the second source/drain region of at least one memory cell (drain terminals of the transistors are connected to bit lines); attaching a single array of parallel wordlines (30-33 in figure 2A) to the gate region of at least one memory cell, the single array of parallel wordlines having a pitch (a space between word lines 31 and 32 in figure 2B); attaching a number of strapping lines (110-115) of lower resistance than the wordlines (column 4, lines 9-11) which bypass portions of the wordlines in the array of parallel wordlines and bypass only a portion of a wordline within the memory cell array (figure 2A shows bypassed strapping lines at two ends or in the middle of a word line) and, wherein at least one portion of a single continuous wordline (31) is only in a middle

region between a first and second end of the single continuous wordline, wherein the strapping lines are each located a distance from each other that is greater than the pitch (figure 2B shows a distance between strapping lines 112 and 113 being greater than the pitch between word lines 31 and 32), and wherein adjacent strapping lines (110 and 112) bypass different portions of adjacent wordlines within the memory cell array; and connecting the strapping lines (112) to the wordlines by forming at least two channels (at nodes such as node 150) from each strapping line to individual wordlines.

Regarding claim 50, Cowles teaches that attaching a number of strapping lines (112, 113) comprises attaching a number of metal strapping lines (column 4, line 9-11).

Regarding claim 51,Cowles teaches that attaching a number of metal strapping lines comprises attaching a number of refractory metal strapping lines (titanium and tungsten are refractory metals; column 4, lines 5-11).

Regarding claim 52, Cowles teaches that attaching a number of strapping lines (110 and 112) comprises attaching the strapping lines on alternating wordlines (30 and 31) in the array.

Regarding claim 53, Cowles teaches that attaching the strapping lines comprises attaching the strapping lines (110, 112) on adjacent wordlines (30, 31) and staggering the strapping lines along the wordlines such that the portions of the adjacent wordlines that are bypassed are not adjacent to each other.

Regarding claim 54, Cowles teaches that attaching a number of strapping lines comprises attaching the strapping lines (110, 111) on a first half portion of a number of

even wordlines in the array and attaching the strapping lines (112, 113) on a second half portion of a number of odd wordlines.

Claims 55-57 are rejected under 35 U.S.C. 102(b) as being anticipated by Cowles (U.S. Patent 5,940,315).

Regarding claim 55, Cowles teaches a memory device comprising: a memory array (comprising arrays 20 and 21 of memory block 100 in figure 2A) including a number of memory cells (not shown); an even row decoder (EVEN) located on a first side (left side) of the memory array; an odd row decoder (ODD) located on a second side (right side) of the memory array; a single column decoder (consisting of COL DEC 40 and 41) connected to the memory array; a number of parallel wordlines (30, 31, 32, 33) local to the memory array coupled to gate regions of memory cells, including one or more even wordlines (30, 32) coupled to the even row decoder, and one or more odd wordlines (31, 33) coupled to the odd row decoder, the odd wordlines arranged alternately with the even wordlines; and a number of strapping lines (110, 111, 112, and 113) having lower resistance than the wordlines (column 4, lines 5-11) and connected to bypass portions of the wordlines within the memory array, wherein a strapping line (112) connected to an odd wordline (31) bypasses only a portion of the odd wordline within the memory array nearer the odd row decoder (ODD), wherein a strapping line (110) connected to an even wordline (30) bypasses only a portion of the even wordline within the memory array nearer the even row decoder (EVEN).

Regarding claim 56, Cowles teaches that the even row decoder (EVEN, 50) is located directly adjacent the first side (left side) and the odd row decoder (ODD, 52) is located directly adjacent the second side (right side).

Regarding claim 57, Cowles teaches a strapping line (112) connected to an odd wordline (31) bypasses only one half of the wordline (from node 150 to row driver circuitry 55 in figure 2A) within the memory array nearer the odd row decoder (ODD, 52) and a strapping line (110) connected to an even wordline (30) bypasses only one half of the wordline (region 20 is one half of the memory array 20 and 21) within the memory array nearer the even row decoder (In this rejection, the regions 20 and 21 is considered as the memory array as claimed.)

(10) Response to Argument

1) Applicable Law

Appellant argues that the Final Office Action did not make out a prima facie case of anticipation because the Cowles patent does not teach each and every claim element arranged as claims. By the principle of inherency under 35 U.S.C. 102, a prior art reference does not expressly show every element to anticipate claims in an application. Where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best,* 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977). "When the PTO shows a sound basis for believing that the products of the applicant and the

prior art are the same, the applicant has the burden of showing that they are not." *In re Spada,* 911 F.2d 705, 709, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990).

2) Discussion of the rejection of claims 1-41 and 45-47 under 35 U.S.C. 102(b) as anticipated by Cowles (U.S. Pat. No. 5,940,315).

Appellant argues that the Final Office Action has not made a proper *prima facie* showing of anticipation. The Examiner would like to direct Appellant to the above paragraph "Where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established."

a. Discussion of the rejection of claims 1- 4, 8-14, 15-18, and 26-29

Appellant argues that Cowles does not show "a number of memory cells," a number of source lines," or "a number of bit lines". As such, the Final Office Action has not made a *prima facie* case of anticipation. On the contrary, since the connections between memory cells, source lines and bit lines are inherent in a semiconductor memory (even the Appellant admits it as Prior Art in figure 4), Cowles only shows in figure 2A, word lines 30-33 where memory cells connected to. Instead Cowles focuses his invention on strapping lines 112, 113 having low resistance to minimize delays in signal propagation through word lines (column 1, lines 57-64). The gist of the instant application and Cowles is about how to reduce signal propagation through word lines to improve a memory device performance, not about connections as argued by Appellant. To further clarify the connection between the memory cells, source lines and bit lines,

the Examiner would like to direct Appellant to Sukegawa et al. (U.S. Patent 5,841,688) cited in the Office Action dated 12/10/2003. Here, Sukegawa is extrinsic evidence. In figure4, Sukegawa shows memory cells 432 connected to transistor 430 through a source line and connected to bit line 334 through the transistor 430.

i.) Discussion of claims 1-4

Appellant alleges that the conductive straps of Cowles bypass a wordline across an entire memory array, not "only a portion of a wordline within a single array" as in claim 1. For the purpose of this rejection, the Examiner considers the arrays 20-23 in figure 2A of Cowles as a single array and the strap line 112 clearly bypass only a middle portion of the word line 31.

ii.) Discussion of claims 8-14

Appellant argues that the Cowles patent does not teach the limitation of claims 8-14. The Examiner believes that all the limitations have been addressed in the above Grounds of Rejection. Cowles discloses a memory device, comprising: a number of memory cells (not shown but inherent in a DRAM device) having a first source/drain region and a second source/drain region and a gate region, the memory cells forming a memory cell array; a number of source lines (not shown but inherent as lines connected to capacitors in a DRAM) coupled to the first source/drain region of at least one memory cell; a number of bit lines (not shown but inherent as bit lines in a DRAM) coupled to the second source/drain region of at least one memory cell; a single array (arrays 20-23 in figure 2A are considered a single array for this rejection) of parallel wordlines (30-33) coupled to the gate region of at least one memory cell (as shown in figure 4 of the

instant application), the array of parallel wordlines having a pitch (space between word lines 31 and 32 in figure 2B); a number of strapping devices (110 to 115 in figure 2A) which bypass portions of the wordlines in the single array of parallel wordlines, wherein at least one portion of a single continuous wordline is only in a middle region (strapping device 112) between a first and second end of the single continuous wordline, and wherein adjacent strapping devices bypass only a portion (strapping device 110) of a wordline within the memory array and bypass different portions of adjacent wordlines within the memory array, each strapping device (110-115) comprising: a strapping line of lower resistance than the wordlines (column 4, lines 9-11), wherein the strapping lines are each located a distance from each other that is greater than the pitch (figure 2B shows a distance between strapping lines 112 and 113 being greater than the pitch between word lines 31 and 32); and at least two channels (at nodes such as node 150 in figure 2A) connecting each strapping line to a portion of a single wordline.

iii.) Discussion of claims 15-18

Appellant argues that the Cowles patent does not teach the limitation of claims 15-18. The Examiner believes that all the limitations have been addressed in the above Grounds of Rejection. Cowles teaches an integrated circuit (figure 2A) comprising: at least one memory array (20-23) comprising: a number of memory cells (not shown but inherent in a DRAM device) having a first source/drain region and a second source/drain region and a gate region; a number of source lines (not shown) coupled to the first source/drain region of at least one memory cell; a number of bit lines

(not shown) coupled to the second source/drain region of at least one memory cell; a number of wordlines (30, 31 in figure 2A) in a single array (arrays 20-23 are considered as a single array) coupled to the gate region of at least one memory cell; a strapping line (112) of lower resistance than the wordlines (column 4, lines 9-11) coupled to a single continuous wordline (31) wherein the strapping line (112) bypasses only a portion of the wordline within the memory array in a middle region between a first and second end of the single continuous wordline, wherein the strapping line (112) is spaced apart from adjacent conductive structures (113 in figure 2B) by a distance greater than a wordline pitch (a space between 112 and 113 is greater than a space between 31 and 32), and wherein the strapping line (112) bypasses a different portion of a wordline within the memory array than an adjacent strapping line (110 or 111 in figure 2A); at least two channels (at nodes such as node 150 in figure 2A) connecting the strapping line to a first and second end of the portion of the single continuous wordline (31); a row decoder (50 in figure 2A); a column decoder (40); and a sense amplifier (column 1, lines 35-38).

iv.) Discussion of claims 26-29

Appellant argues that the Cowles patent does not teach the limitation of claims 26-29. The Examiner believes that all the limitations have been addressed in the above Grounds of Rejection. Cowles shows in figure 3, information handling device comprising: a processing unit (334); at least one memory array (348). Cowles also teaches an integrated circuit (figure 2A) comprising: at least one memory array (20-23) comprising: a number of memory cells (not shown but inherent in a DRAM device)

having a first source/drain region and a second source/drain region and a gate region; a number of source lines (not shown) coupled to the first source/drain region of at least one memory cell; a number of bit lines (not shown) coupled to the second source/drain region of at least one memory cell; a number of wordlines (30, 31 in figure 2A) in a single array (arrays 20-23 are considered as a single array) coupled to the gate region of at least one memory cell; a strapping line (112) of lower resistance than the wordlines (column 4, lines 9-11) coupled to a single continuous wordline (31) wherein the strapping line (112) bypasses only a portion of the wordline within the memory array in a middle region between a first and second end of the single continuous wordline, wherein the strapping line (112) is spaced apart from adjacent conductive structures (113 in figure 2B) by a distance greater than a wordline pitch (a space between 112 and 113 is greater than a space between 31 and 32), and wherein the strapping line (112) bypasses a different portion of a wordline within the memory array than an adjacent strapping line (110 or 111 in figure 2A); at least two channels (at nodes such as node 150 in figure 2A) connecting the strapping line to a first and second end of the portion of the single continuous wordline (31); a row decoder (50 in figure 2A); a column decoder (40); and a sense amplifier (column 1, lines 35-38).

b. Discussion of the rejection of claims 5-7, 19-25, 30-36, 37-41, 45-48, and 49-54

i.) Discussions of claims 5-7

Appellant argues that the Cowles patent does not teach the limitation of claims 5-7. Appellant alleges that the conductive straps of Cowles bypass a wordline across an entire memory array, instead of "only a portion of a wordline within the memory array" as recited in claim 5. For the purpose of this rejection, the Examiner considers the arrays 20-23 in figure 2A of Cowles as a single array and the strap line 112 clearly bypass only a middle portion of the word line 31.

ii.) Discussions of claims 19-25

Appellant argues that the Cowles patent does not teach the limitation of claims 19-25. The Examiner believes that all the limitations have been addressed in the above Grounds of Rejection. Cowles teaches an integrated circuit (figure 2A) comprising: at least one memory array (memory bank 100) comprising: a number of memory cells (not shown) having a first source/drain region and a second source/drain region and a gate region; a number of source lines coupled to the first source/drain region of at least one memory cell; a number of bit lines coupled to the second source/drain region of at least one memory cell; a single array of parallel wordlines (30-33) coupled to the gate region of at least one memory cell, the array of parallel wordlines having a pitch (space between word lines 31 and 32 in figure 2B); a number of separate strapping devices (110-115) which bypass separate portions of a single continuous wordline in the single array of parallel wordlines, and wherein adjacent strapping devices (110 and 112) bypass only a portion of a wordline within the memory array and bypass different portions of adjacent wordlines within the single array, each strapping device (110-115) comprising: a strapping line of lower resistance than the

wordlines (column 4, lines 5-11), wherein the strapping lines are each located a distance from each other that is greater than the pitch (figure 2B shows a distance between strapping lines 112 and 113 being greater than the pitch between word lines 31 and 32); and at least two channels (at nodes such as node 150 in figure 2A) connecting the strapping line to the single continuous wordline (31); a row decoder (50); a column decoder (40); and a sense amplifier (column 1, lines 35-38).

iii.) Discussions of claims 30-36

Appellant argues that the Cowles patent does not teach the limitation of claims 30-36. The Examiner believes that all the limitations have been addressed in the above Grounds of Rejection. Cowles teaches information handling device (figure 3) comprising: a processing unit (344); at least one memory array (348). Cowles also teaches an integrated circuit (figure 2A) comprising: at least one memory array (memory bank 100) comprising: a number of memory cells (not shown) having a first source/drain region and a second source/drain region and a gate region; a number of source lines coupled to the first source/drain region of at least one memory cell; a number of bit lines coupled to the second source/drain region of at least one memory cell; a single array of parallel wordlines (30-33) coupled to the gate region of at least one memory cell, the array of parallel wordlines having a pitch (space between word lines 31 and 32 in figure 2B); a number of separate strapping devices (110-115) which bypass separate portions of a single continuous wordline in the single array of parallel wordlines, and wherein adjacent strapping devices (110 and 112) bypass only a portion of a wordline within the memory array and bypass different portions of adjacent wordlines within the single

array, each strapping device (110-115) comprising: a strapping line of lower resistance than the wordlines (column 4, lines 5-11), wherein the strapping lines are each located a distance from each other that is greater than the pitch (figure 2B shows a distance between strapping lines 112 and 113 being greater than the pitch between word lines 31 and 32); and at least two channels (at nodes such as node 150 in figure 2A) connecting the strapping line to the single continuous wordline (31); a row decoder (50); a column decoder (40); and a sense amplifier (column 1, lines 35-38).

iv.) Discussions of claims 37-41

Appellant argues that the Cowles patent does not teach the limitation of claims 37-41. The Examiner believes that all the limitations have been addressed in the above Grounds of Rejection. Cowles discloses a method of reducing a wordline RC time constant (to minimize signal delays; column 1, lines 57-64) comprising: spacing a number of strapping devices (110-115 in figure 2A) over wordlines (30-33) within a single memory array (memory bank 100) apart from adjacent strapping devices by a distance greater than a wordline pitch (figure 2B shows a distance between strapping lines 112 and 113 being greater than the pitch between word lines 31 and 32), wherein adjacent strapping devices bypass different portions of adjacent wordlines within the single memory array; connecting individual strapping devices (112 and 113) to portions in a middle region between a first and second end of single continuous wordlines (31 and 33) using at least two channels (at nodes 150) for each strapping device; activating a first number of transistors (transistors of memory cells connected to word line 31 in regions 21 and 22) coupled to a first portion of a wordline; and activating a second

number of transistors (transistors of memory cells connected to the word line 31 in regions 20 and 23) coupled to a second portion of a wordline, wherein a signal used for activating the second number of transistors bypasses the first portion of the wordline through a strapping device of lower resistance than the first portion of the wordline (column 4, lines 12-19); activating a selected bitline in the memory array associated with a selected memory cell (column 1, lines 32-38); discharging the selected memory cell through a selected transistor, the selected transistor being activated by both the selected row and the selected bitline (column 1, lines 32-38); and sensing the presence or absence of a charge from the selected memory cell through the use of a sense amplifier (column 1, lines 32-38).

v.) Discussions of claims 45-48

Appellant argues that the Cowles patent does not teach the limitation of claims 45-48. The Examiner believes that all the limitations have been addressed in the above Grounds of Rejection. Cowles teaches a method of forming a memory device (figures 2A and 2B) comprising: forming a number of memory cells (not shown but understood as inherent in a semiconductor memory device; column 3, lines 22-33) having a first source/drain region and a second source/drain region and a gate region (such as a memory cell shown in figure 4 of the instant application), the memory cells forming a memory cell array (figure 2A); coupling a number of source lines to the first source/drain region of at least one memory cell (source terminals of transistors in figure 4 of the instant application are connected to a source line); coupling a number of bit lines to the second source/drain region of at least one memory cell (drain terminals of

the transistors are connected to bit lines); attaching a number of wordlines to the gate region of at least one memory cell to form a single array (gate terminals of the transistors are connected to word lines); attaching a strapping line (112 in figure 2A) of lower resistance than the wordlines (column 4, lines 9-11) to a single continuous wordline (31 in figure 2A) wherein the strapping line bypasses only a portion in a middle region between a first and second end of the single continuous wordline, wherein the strapping line (112) is spaced apart from adjacent conductive structures (113) by a spacing greater than a wordline pitch (figure 2B shows a distance between strapping lines 112 and 113 being greater than the pitch between word lines 31 and 32) and wherein the strapping line (112) bypasses only a portion of a wordline within the memory cell array and bypasses a different portion of a wordline within the memory cell array than an adjacent strapping line (110 or 111); and connecting the strapping line (112) to the single wordline (31) by forming at least two channels (at nodes such as 150) from the strapping line to the single continuous wordline.

vi.) Discussions of claims 49-54

Appellant argues that the Cowles patent does not teach the limitation of claims 49-54. The Examiner believes that all the limitations have been addressed in the above Grounds of Rejection. Cowles teaches a method of forming a memory device (figure 2A) comprising: forming a number of memory cells (not shown but understood as inherent in a semiconductor memory device; column 3, lines 22-33) having a first source/drain region and a second source/drain region and a gate region (such as a memory cell shown in figure 4 of the instant application), the memory cells forming a

memory cell array (figure 2A); coupling a number of source lines coupled to the first source/drain region of at least one memory cell (source terminals of transistors in figure 4 of the instant application are connected to a source line); coupling a number of bit lines coupled to the second source/drain region of at least one memory cell (drain terminals of the transistors are connected to bit lines); attaching a single array of parallel wordlines (30-33 in figure 2A) to the gate region of at least one memory cell, the single array of parallel wordlines having a pitch (a space between word lines 31 and 32 in figure 2B); attaching a number of strapping lines (110-115) of lower resistance than the wordlines (column 4, lines 9-11) which bypass portions of the wordlines in the array of parallel wordlines and bypass only a portion of a wordline within the memory cell array (figure 2A shows bypassed strapping lines at two ends or in the middle of a word line) and, wherein at least one portion of a single continuous wordline (31) is only in a middle region between a first and second end of the single continuous wordline, wherein the strapping lines are each located a distance from each other that is greater than the pitch (figure 2B shows a distance between strapping lines 112 and 113 being greater than the pitch between word lines 31 and 32), and wherein adjacent strapping lines (110 and 112) bypass different portions of adjacent wordlines within the memory cell array; and connecting the strapping lines (112) to the wordlines by forming at least two channels (at nodes such as node 150) from each strapping line to individual wordlines.

c. Discussion of the rejection of claims 55-57

Appellant alleges that the Cowles patent fails to teach the limitations of claim 55-57. The conductive straps of Cowles bypass a wordline across an entire memory array, instead of only "portions of the wordlines within the memory array" as recited in claim 55. This allegation is not correct because Cowles shows in figure 2A, the strap line 112 consisting of two portions joining each other at row drive circuitry 55. Each portion of the strap line 112 bypasses a portion of the wordline 31, in other words, the portions of the strap line 112 bypass portions of the wordlines when many wordlines are under consideration.

Appellant further argues that "Cowles refers to an arrangement where an even row decoder is on one side of two memory arrays and an odd row decoder is on an opposite side of the two memory arrays, and therefore Cowles does not describe the structure recited in claim 55." In the rejection of claim 55, two arrays 20 and 21 are considered as one array; and the even and odd row decoders are clearly shown as even row decoder 50 and odd row decoder 52.

d. Conclusion

By the principle of inherency, the prima facie case of anticipation is met. An extrinsic evidence to memory cells, source lines, and bit lines is demonstrated by Sukegawa et al. (U.S. Patent 5,841,688) cited in the Office Action dated 12/10/2003. Therefore, claims 1-41 and 45-57 should be rejected under 35 U.S.C. 102(b) as being anticipated by Cowles (U.S. Patent 5,940,315).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Son Mai

SON L. MAI
PRIMARY EXAMINER

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